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(56) Documents Cited:
EP 0593922 A1
US 5051832 A
US 4649554 A
US 5710447 A
US 4866496 A

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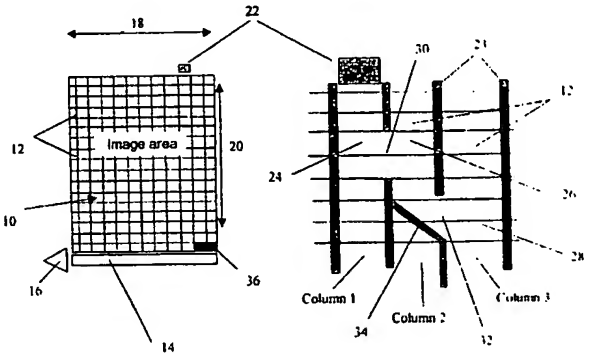
(54) Abstract Title: **Solid state imager**

(57) A charge division arrangement for a CCD device for producing a divided charge output from an input charge, comprising an input for receiving an input charge, an array of elements and an output. The array of elements being arranged in rows and columns and having clock connections to allow charge in each row to be successively clocked from one row of elements to the next. At least some of the elements being arranged in a charge division unit having a first element and a second element in adjacent columns and being communicable at least temporarily so that charged introduced into the first element is divided between the first element and the second element, the charge division unit being arranged to produce divided charge for production at the output. The arrangement allows a small amount of charge to be introduced into a CCD circuit.

Fig 1



GB 2 395 068 A

Fig 2

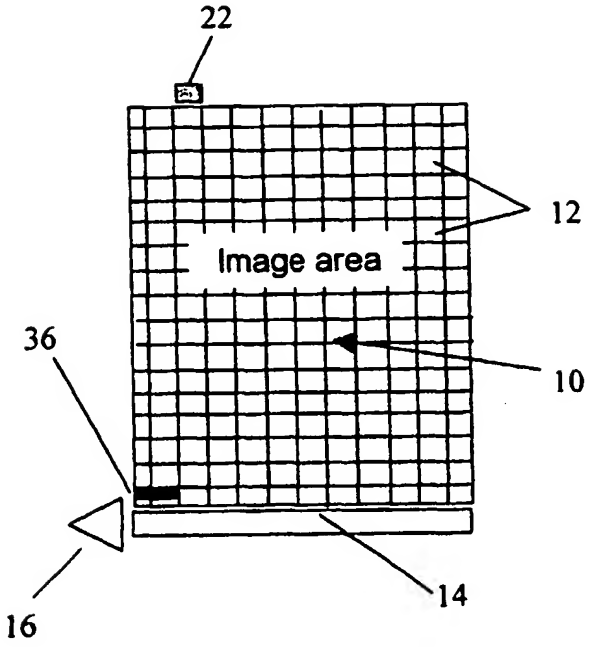
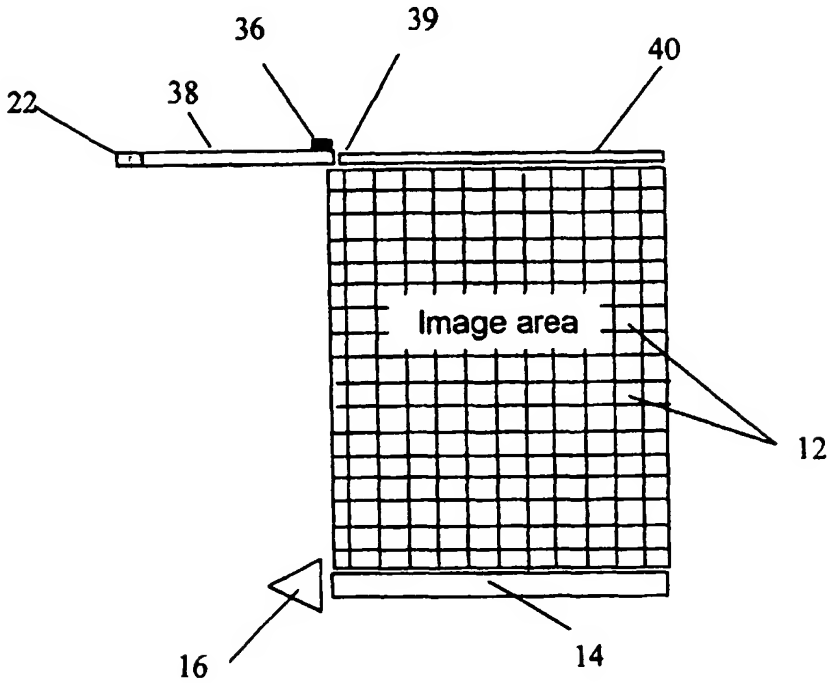


Fig 3



SUMMARY OF THE INVENTION

We have appreciated the need for introduction of a known level of charge into a CCD circuit for various purposes, such as for calibration of the output circuit, for example, or as a mechanism to avoid the effects of electron capture as a result of proton or neutron damage. We have further appreciated, however, that it is difficult to controllably inject appropriate amounts of charges less than around 10,000 electrons.

The invention is defined in the claims to which reference is now directed with preferred features set out in the dependent claims.

The invention may be embodied in two ways. In the first way, some elements within a CCD imager have isolation regions or barriers between columns that are selectably removable. This allows charge introduced into a first row of the imager to be clocked to successive rows and for charge to be divided between one column and another as it progresses through the rows. This allows a defined divided charge to be presented at an output of the device for input to an output circuit.

Alternatively a permanently enabled splitting structure may be incorporated in additional columns at the side of the array which are shielded from incident illumination. In the second embodiment, a charge division structure as described is provided in addition to, and at an input of, the CCD imager. This allows a defined divided charge to be input to the imager.

In either embodiment, a small charge may be injected into a final output register. One application of this is to introduce a "fat zero" which is a small charge level in

circuit 16 for purposes such as calibration. Known techniques involve injecting charge directly into the serial register. In the present embodiment, however, charge is injected into a first row of the CCD imager image area 10 denoted as position 22. The charge injected at position 22 is sequentially transferred from one row to another down through the image area 10 to the serial register14. We have appreciated that use can be made of the clocking of charge from one row to another to provide for division of that charge and thereby to allow small defined elements of charge to be injected from the image area 10 to the serial register 14. Transfer and division can occur automatically as part of a normal signal readout sequence or in a special non-image acquisition mode. The arrangement for charge division is shown on the right-hand side of the Figure 1.

Three columns of the array 10 are shown in greater detail on the right-hand side of Figure 1 showing an array of elements 12 with column isolation barriers 23 between them. The configuration of adjacent rows and columns as shown comprises a charge division unit, which is configured so that charge introduced at the injection position 22 can be divided in the sense that a portion of the charge diverted elsewhere. Such division is preferably integer division, but could equally be non-integer division depending upon the relative areas of charge storage in columns 1 and 2 defined within the structure. The division unit comprises a first element 24 in a first column adjacent a second element 26 in a second column. Ordinarily, a column isolation barrier 23 would be present between the elements 24 and 26. However, when operating according to the invention, the barrier between the first element 24 and second element 26 is removed, shown as position 30, which allows charge to flow from position 24 to 26. In the event that the barrier is removed at position 30, the charge at positions 24 and 26

In the simple case shown of having a removable barrier between two columns, the simplest case is division of charge by two. By providing a plurality of such division units within the image area structure, significant charge division can be obtained (by repeatedly dividing the charge by two at each unit). Although the example of a removable barrier between two columns is shown, it may be possible to extend the concept to have removable barriers between more columns to increase the charge division at each charge division unit. For example, removable barriers between three columns would allow charge to be divided by three when charge is clocked to the relevant position and the isolation columns removed at that position. Other removable barrier arrangements are possible and will depend upon the clock speed at which charges clocked from one row to another. The use of the selectable barrier at positions 32 and 34 is preferred to allow excess charge to be removed from column 2. If this barrier were not present within each division unit, charge at position 26 would simply be clocked down column 2 such that it would remain adjacent the charge at position 24 when clocked from one row to another. As a result, charge would not then flow from column 1 to column 2 - the charge being equal in both.

In the embodiment in Figure 1, the charge is injected at a column, three columns from the end of the structure and, in particular, three columns from the dump diode 36. As a result, charge is injected to the register at a position three columns from the right-hand end, being the end removed from the output circuit 20. The excess charge from column 3 is passed out through the diode 36.

An alternative embodiment is shown in Figure 2 using the same arrangement of division units of elements within the image area, but having a charge injection position 22 near the left-hand end of the series of columns, namely at a

which would then transfer injected charge into selected columns of the main array 10. Using the charge distribution register allows charge to be injected so that, when transferred down through the rows of the image area 10, it appears at the end of the serial register distant from the output circuit in a similar manner to that shown in Figure 1, or to be injected into the image area 10 so as to appear at the output circuit 20 without the requirement to be clocked through the serial register 14. Of course, charge could also be injected at any position between these two.

In common with the embodiments of either Figure 1, 2 or 3 is that various elements within an array of elements or cells are arranged so that, as charge is clocked from one row to another, charge can be divided from one column to another by use of either permanently removed or selectively removable isolation regions between columns. In the case of such arrangement of elements described as division units within the main image area 10, the regions between columns which control the division of charge needs to be selectively removable (or controllable generally in height) so that the barrier regions are in place when the array is in a normal image acquisition mode. Otherwise, there would be a blurring of charge and hence a blurring of the resultant image. In a charge injection mode in which charge is to be divided through the array, the barriers are reduced or removed. In the embodiment of Figure 3, or where the division structure is incorporated in additional columns at the side of the image array, the barrier regions may also be selectively removable, but of course could also be permanently fixed as present or absent (or a position between depending upon the division ratio) as the charge division structure does not also need to function as an image acquisition area.

CLAIMS

1. A charge division arrangement for a CCD device for producing a divided charge output from an input charge, comprising an input for receiving an input charge, an array of elements and an output, the array of elements being arranged in rows and columns and having clock connections to allow charge in each row to be successively clocked from one row of elements to the next, at least some of the elements being arranged in a charge division unit having a first element and a second element in adjacent columns and being communicable at least temporarily so that charged introduced into the first element is divided between the first element and the second element, the charge division unit being arranged to produce divided charge for production at the output.

2. A charge division arrangement according to claim 1, comprising a plurality of charge division units, the output of one charge division unit being arranged to provide charge to the first element of a subsequent charge division unit.

3. A charge division arrangement according to claim 1 or 2, wherein the or each charge division unit comprises three elements, the first element and second element in adjacent columns and being communicable at least temporarily, a third element in a column adjacent to the second element and arranged to receive charge from the second element.

4. A charge division arrangement according to claim 3 when appendant claim 2, wherein the first element of each charge division unit is arranged to receive charge from the first element of a previous charge division unit.

12

Application No:	GB 0323200.6	**Examiner:**	Lars Kjer Pedersen
Claims searched:	1-10	**Date of search:**	2 March 2004

Patents Act 1977 : Search Report under Section 17

Documents considered to be relevant:

Category	Relevant to claims	Identity of document and passage or figure of particular relevance	
A	1-10	EP 0593922 A1	(SONY) whole document
A	1-10	US 5710447 A	(TOHYAMA) whole document
A	1-10	US 5051832 A	(LOSEE) whole document
A	1-10	US 4866496 A	(AUDIER) whole document
A	1-10	US 4649554 A	(BOUDEWIJNS) whole document

Categories:

X	Document indicating lack of novelty or inventive step	A	Document indicating technological background and/or state of the art
Y	Document indicating lack of inventive step if combined with one or more other documents of same category	P	Document published on or after the declared priority date but before the filing date of this invention
&	Member of the same patent family	E	Patent document published on or after, but with priority date earlier than, the filing date of this application

Field of Search:

Search of GB, EP, WO & US patent documents classified in the following areas of the UKC[W]

Worldwide search of patent documents classified in the following areas of the IPC[7]:

H01L

The following online and other databases have been used in the preparation of this search report:

EPODOC, WPI, JAPIO